13.6 A 10Gb/s Burst-Mode/Continuous-Mode Laser Driver with Current-Mode Extinction-Ratio Compensation Circuit

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PONs are being investigated as an effective way for high-speed communications. These packet-based systems require burst-mode transmitters. In such transmitters, a driver is designed to modulate the laser output for each packet. Previous Gb/s burst-mode drivers [1] only applied single-loop automatic power control (APC) circuits to fix the laser power. However, it is not adequate to maintain the extinction ratio (ER) and the signal fidelity degrades when the laser diode experiences a temperature rise or aging effect. Another previous 155Mb/s burst-mode driver [2] is only applicable to asynchronous transfer mode based PON (APON). Since a 10Gb/s laser diode (LD) is expensive, it is desired to prolong its life. In this paper, a 10Gb/s burst-mode/continuous-mode laser driver with dual-loop current-mode APC in 0.18μm CMOS process is described. The driver can automatically compensate the ER of the laser output under continuous-mode or under burst-mode operation with laser turn on/off time less than 3ns. Figure 13.6.1 shows a block diagram of the driver. The driver comprises a differential cascode gain stage, an LD, a monitor photodiode (PD), a regulated-cascode TIA (RGC-TIA), a pair of peak/bottom detectors, an offset-voltage generator, several voltage-to-current (V/I) converters, two pairs of switches controlled by a burst-enable (B_EN) signal, and two current comparators C1 and C2 for respectively controlling laser bias current I_{BIAS} and modulation current I_{MOD}. To generate a large output swing for driving LDs, a local feedback technique (IDGCFN) is used [3]. The high and low optical power level, P_1 and P_0, are related to the detected levels, V_H and V_L, as (1) and (2) in Fig. 13.6.1, with R the responsivity, R_f the gain of the RGC-TIA, and V_{th} the offset level when there is no PD current (I_{off} = 0). The idea is to convert the detected voltage levels into currents and make use of C1 and C2 to implement (3) and (4) to control I_{BIAS} and I_{MOD}, respectively. ΔV in (3) is a reference value. From (5), the ER (= K + 1) could be independent of process and temperature variations, if K is implemented by a CMOS current mirror.

Figure 13.6.2 shows the RGC-TIA with a monitor PD modelled by a parasitic resistor R_{PD}, a capacitor C_{PD}, and a current source I_{PD}. Simulated frequency responses of the TIA with various PDs show that the -3dB bandwidth of the monitor PD in a commercial 10Gb/s laser module is usually much smaller than 2GHz (C_{PD} = 7pF). For optical tests, the driver ICs are integrated with commercial 1310nm InGaAs PDs in chip-on-board (COB) assemblies. The active area of the PD is 70μm in diameter. The reverse bias voltage applied to the PD is about 1V and its parasitic capacitance is about 0.7pF. The corresponding -3dB bandwidth is greater than 3GHz. The responsivity of the PD is 0.9A/W. Figure 13.6.2 also shows simulated $V_H - V_L$ versus the amplitude of I_{PD} with I_{BIAS} fixed and a K28.5 NRZ input stream applied. It clearly shows that with 5 consecutive "1"s (or "0"s) the level difference curves could reach to their peak values. For a usual commercial laser module, level detectors can not reach their peak values unless an almost no R_{PD} PD is used.

Figure 13.6.3 shows a traditional and a low-voltage V/I converters. To minimize the effect of the noise and the voltage droop on V_H and V_L, the output swing of TIA is designed as large as possible. However, the input dynamic range of the traditional V/I converter is small. The output of the V/I converter may saturate and therefore the control loops lock to the wrong points. Moreover, it is not easy to design a proper V/I converter with sufficient headroom under a small supply voltage. And the traditional V/I converter needs two additional opamps and increases the power consumption. To solve the problem, a low-voltage V/I converter is used, as shown in Fig. 13.6.3. K is the output current ratio. Simulated V/I transfer curve shows that its input dynamic range is very wide with a negligible offset voltage.

Figure 13.6.4 shows the block diagrams of comparators C1 and C2. In C1, V_{refL} is a fixed voltage, and V_{refH} is set by the user to implement ΔV (= $V_{refH} - V_{refL}$) in (3) in Fig. 13.6.1. In C2, the current ratio of the V/I converters with input V_{refL} and V_{refH} are set to be $K = ER - 1$ to implement (4).

Figure 13.6.5 shows the measurement setup. The test board is placed on an x-y stage. The driver directly modulates a commercial 1310nm MQW-DFB LD. To automatically compensate the ER, the LD is connected with an 80/20 power splitter to feedback 20% of the output power to the PD through a fiber probe. The other branch of the splitter is connected to an O/E converter. The pattern generator sends a K28.5 pattern as the input data and its trigger output is connected to the function generator for generating the signal B_EN. Timing diagrams are shown on the oscilloscope. To obtain the electrical timing diagrams, the output of the driver is dc-coupled to the oscilloscope. The electrical timing diagrams show that the modulation current switching delay is less than 1ns. The optical timing diagram shows that the laser turn on/off time is 15.5ns – $2/v_f$ – $0.7/v_c$ = 2.4ns, where v_f (= 1.97×10^8ms^{-1}) and v_c (= 2.31×10^8ms^{-1}) represent the propagation velocities on the fiber and the cable respectively.

Figure 13.6.6 shows the measured and predicted ERs versus I_{BIAS}. The threshold current of the LD is about 10mA with laser efficiency η_d = 0.034W/A at T = 25°C. It decreases to 8mA with η_d = 0.038W/A at T = 0°C and increases to 20mA with η_d = 0.026W/A at T = 85°C. The target ER is designated as 6dB, and therefore the current ratio is $K = ER - 1 = 3$. The measured ER gets closer to the target value as I_{BIAS} increases. Although the error of the level detectors gets larger and makes the APC lock to a larger ER as I_{BIAS} decreases, the measured optical eye diagrams (16mA < I_{BIAS} < 29mA, or equivalently, 38mA < I_{MOD} < 80mA) stay well within the 10Gb/s Ethernet transmitter mask. The predicted ERs at T = 0°C and T = 85°C are also shown (Fig. 13.6.6). At T = 85°C, I_{BIAS} is greatly increased to maintain the ER owing to the degradation of the laser efficiency. The corresponding I_{MOD} is about 100mA.

Figure 13.6.7 shows the die micrograph of the driver and the performance summary. The driver occupies a die area of $1038\times1040\mu m^2$. It can generate a 20 to 100mA modulation current and a 0 to 80mA bias current, and the power it consumes at T = 25°C with I_{BIAS} = 25mA and I_{MOD} = 68mA is 540mW from a 1.8V supply, including another 4.5V supply for driving the LD.

References:

[1] D. U. Li, L. R. Huang, and C. M. Tsai, "A 3.5-Gb/s CMOS Burst-Mode Laser Driver with Automatic Power Control Using Single Power Supply," *ISCAS Dig. Tech. Papers*, pp. 5501-5504, May, 2005.

[2] Bauwelinck, *et al.*, "Generic and Intelligent CMOS 155Mb/s Burst Mode Laser Driver Chip Design and Performance," *Dig. ESSCIRC*, pp. 495-498, Sept., 2002.

[3] D. U. Li and C. M. Tsai, "10-13.6 Gbit/s 0.18μm CMOS Modulator Drivers with Differential 8 V_{PP} Output Swing," *IEE Electronics Letters*, vol. 41, no. 11, pp. 643-644, May, 2005.

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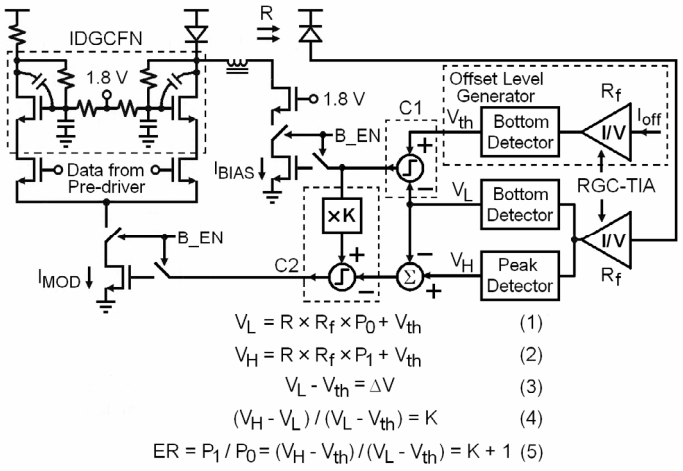

Figure 13.6.1: Block diagram of laser driver.

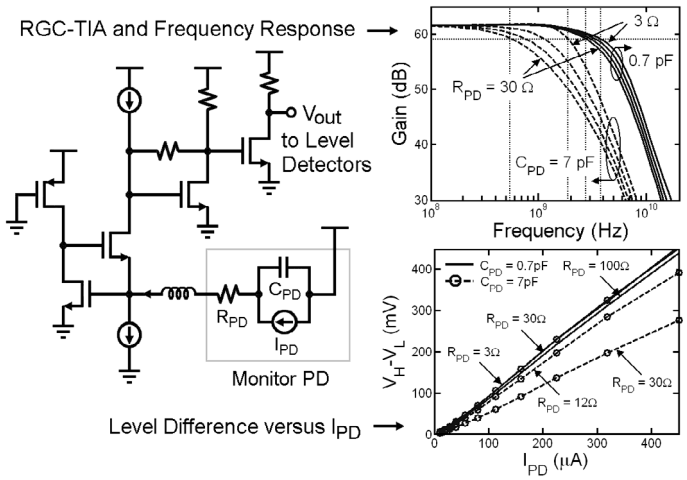

Figure 13.6.2: RGC-TIA with a PD, its frequency response, and V_H–V_L versus amplitude of I_{PD}.

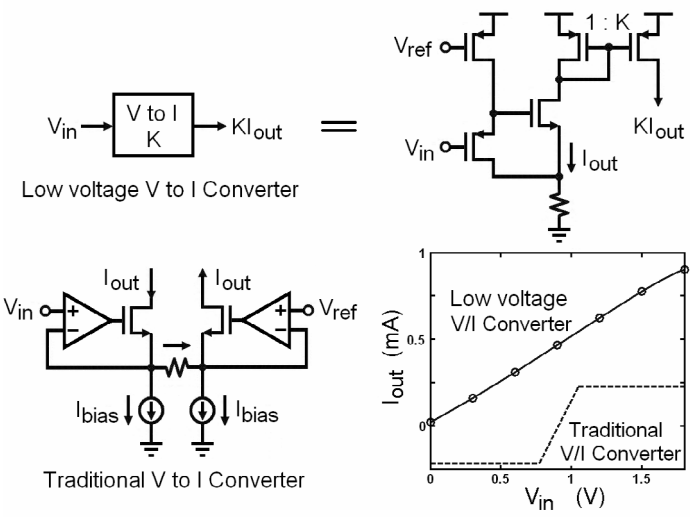

Figure 13.6.3: Traditional and low-voltage V/I converters.

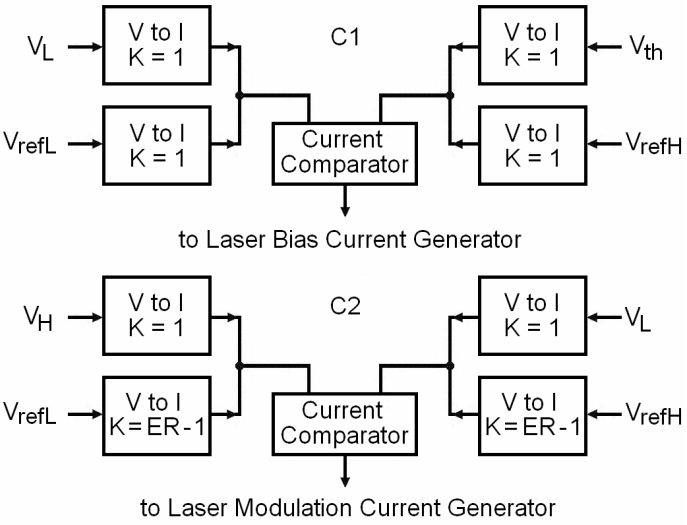

Figure 13.6.4: Block diagrams of comparators C1 and C2.

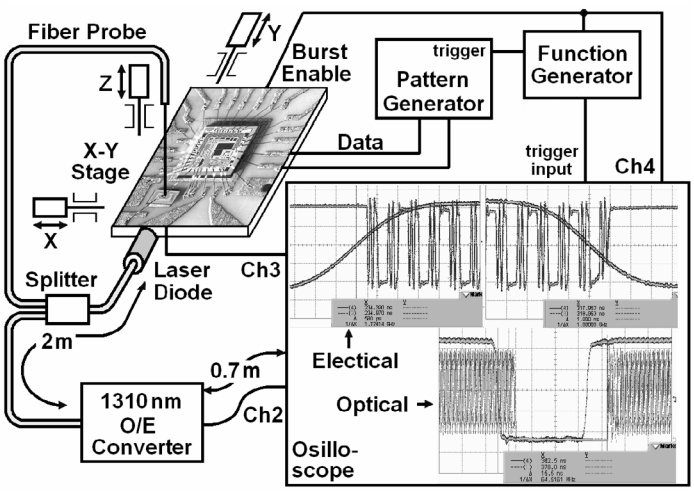

Figure 13.6.5: Measurement setup and measured electrical and optical timing diagrams.

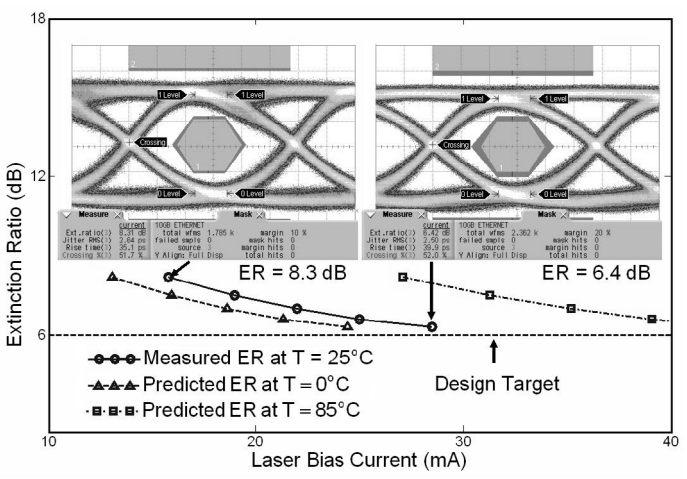

Figure 13.6.6: Measured and predicted ERs versus laser bias current and corresponding optical eye diagrams.

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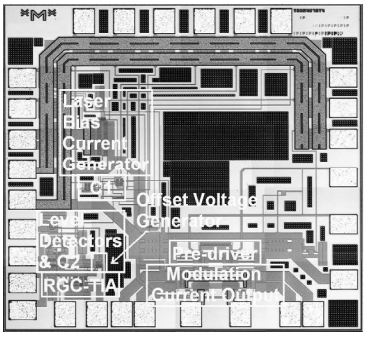

Specification	Value
Data Rate	10Gb/s
Supply Voltage	1.8/4.5V
I_{MOD} Range	20 to 100mA
I_{BIAS} Range	0 to 80mA
Edge Speed (20%-80%)	28/29ps I_{MOD} = 100mA
pk-pk Jitter	6.23ps Measured on
Random Jitter	0.93ps K28.5 Pattern
I_{MOD} Switching Delay	1ns
Laser Turn on/off Time	< 3ns
Output Swing	2.6V Load = 25Ω
Die Size	1038×1040μm²
Technology	0.18μm CMOS
Power Dissipation	0.54W I_{BIAS} = 25mA, I_{MOD} = 68mA

Figure 13.6.7: Die micrograph and performance summary.

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